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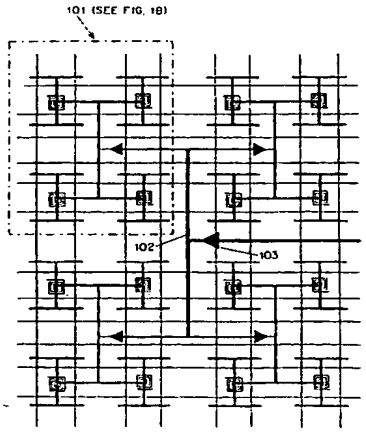
(54) Title: RESONANT CLOCK DISTRIBUTION FOR VERY LARGE SCALE INTEGRATED CIRCUITS



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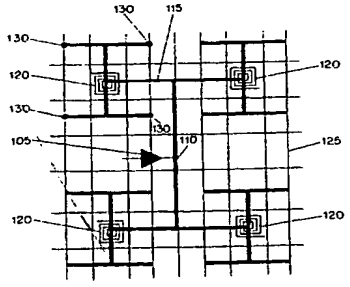

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(57) Abstract: A circuit for distributing a clock signal in an integrated circuit includes a capacitive clock distribution circuit (102) having at least conductor (115) therein. At least one inductor is formed in a metal layer of the integrated circuit and is coupled to the clock distribution circuit. The inductor, generally in the form of a number of spiral inductors (120) distributed throughout the integrated circuit, provides an inductance value selected to resonate with the capacitive clock distribution circuit at resonance, power dissipation is reduced while skew and jitter performance can be improved.

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